Claims:

1. A method of reducing the size of microscratches in a microelectronic device substrate, the method comprising

providing a microelectronic device substrate comprising a surface that includes microscratches,

reducing the size of microscratches by a method comprising

providing pressure and relative movement between the substrate and a polishing pad,

with application of aqueous liquid, and

without application of abrasive particles,

to provide a polished surface having an average density of microscratches having a depth up to 0.5 micron, of less than 1 such microscratch per 100 square microns.

2. The method of claim 1 wherein the polished surface has an average density of microscratches having a depth in the range from 0.001 to 0.1 micron, of less than 1 such microscratch per 100 square microns.

3. The method of claim 1 wherein the polished surface has an average density of microscratches having a depth in the range from 0.2 nanometers to 0.1 microns, of less than 1 such microscratch per 100 square microns.

4. The method of claim 1 wherein the polished surface has an average density of microscratches having a depth in the range from 0.2 nanometers to 0.5 microns, of less than 1 such microscratch per 100 square microns.

5. The method of claim 1 wherein the microscratches of the polished surface have widths in the range from 0.01 to 0.05 micron.

6. The method of claim 1 wherein the microscratches of the polished surface have

a depth up to 0.1 micron,

a width up to 0.05 micron, and

a length up to 10 microns.

7. The method of claim 1 comprising processing a surface of the substrate by chemical-mechanical planarization, followed by reducing the size of microscratches by a method comprising providing pressure and relative movement between the substrate and polishing pad, in the presence of aqueous liquid consisting of water.

8. The method of claim 1 wherein the microelectronic device substrate is a planarized semiconductor wafer.

9. The method of claim 8 wherein the semiconductor wafer is a planarized silicon wafer.

10. The method of claim 1 wherein the polishing pad comprises felt, polymer impregnated felt, polymer, animal hair, or combinations thereof.

11. The method of claim 1 wherein

the surface is polished using a rotating polishing pad and a rotating substrate, and

the pressure between the polishing pad and substrate is in the range of 0.2 to 3 pounds per square inch.

12. The method of claim 11 wherein

the polishing pad has a diameter in the range from 18 to 28 inches, and is rotated at a speed of from 100 to 200 revolutions per minute, and

the substrate has a diameter in the range from 4 to 8 inches, and is rotated at a speed of from 50 to 100 revolutions per minute.

13. The method of claim 1 wherein

the aqueous liquid consists of water, and

the processed surface includes no detectable microscratches having dimensions of a depth in the range from 1 nanometer to 0.1 microns.

14. The method of claim 13 wherein the water is selected from the group consisting of a purified water, a deionized water, a distilled water, a filtered water, and mixtures thereof.

15. The method of claim 1 wherein

the microelectronic device substrate comprises a planarized silicon wafer, and

the method comprises further processing the substrate by providing a component of a magnetoresistive memory device at a substrate surface.

16. The method of claim 15 wherein the component is a component of a giant magneto resistive device.

17. A method of processing a microelectronic device, the method comprising

processing a surface of the semiconductor wafer by chemical-mechanical planarization to produce a planarized surface that contains microscratches,

polishing the planarized surface by a method comprising

providing pressure and relative movement between the substrate and a polishing pad, the pressure between the polishing pad and substrate in the range of 0.2 to 3 pounds per square inch,

in the presence of an applied aqueous liquid, and

in the absence of applied abrasive particles.

18. The method of claim 17 wherein the substrate, having a diameter in the range from 4 to 8 inches, is rotated at a speed in the range from 50 to 100 revolutions per minute.

19. The method of claim 18 wherein

the pad, having a diameter in the range from 18 to 28 inches, is rotated at a speed in the range from 100 to 200 revolutions per minute,

for a total time of from about 1 to about 3 minutes.

20. The method of claim 19 wherein the polished surface includes on average fewer than 1 microscratch per 100 square microns, the microscratches having dimensions of

a depth no greater than 0.1 micron,

a width no greater than 0.05 micron, and

a length no greater than 10 microns.

21. The method of claim 20 wherein

the aqueous liquid consists of water, and

the force between the polishing pad and substrate is in the range of 0.2 to 2 pounds per square inch.

22. The method of claim 20 wherein

the substrate, having a diameter in the range from 4 to 8 inches, is rotated at a speed in the range from 50 to 100 revolutions per minute.

the polishing pad, having a diameter in the range from 18 to 28 inches, is rotated at a speed of from 100 to 200 revolutions per minute, and

the substrate is polished for a total time of from about 1 to about 3 minutes.

23. A microelectronic device substrate comprising a surface having an average density of less than 1 microscratch per 100 square microns.

24. The substrate of claim 23 comprising a surface having an average density of microscratches having a depth in the range from 0.2 nanometers to 0.5 microns, of less than 1 such microscratch per 100 square microns.

25. The substrate of claim 24 wherein the microscratches have a depth of no greater than 0.1 micron.

26. The substrate of claim 23 comprising a surface that includes no detectable microscratches of a depth in the range from 0.2 nanometer to 0.1 micron.

27. The substrate of claim 26 wherein the substrate is a semiconductor wafer.

28. A giant magnetoresistive memory device comprising the semiconductor wafer substrate according to claim 23.